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Steensgaard-Madsen, Jesper; Moon, Un-Ku; Temes, Gabor C.

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MISMATCH-SHAPING SERIAL DIGITAL-TO-ANALOG CONVERTER

Jesper Steensgaard

The Technical University of Denmark
Department of Information Technology
DK–2800, Lyngby, Denmark

Un-Ku Moon and Gabor C. Temes

Oregon State University,
Department of Electrical Engineering,
ECE-220, Corvallis, OR 97331-3211

ABSTRACT

A simple but accurate pseudo-passive mismatch-shaping D/A converter is described. A digital state machine is used to control the switching sequence of a symmetric two-capacitor network that performs the D/A conversion. The error caused by capacitor mismatch is uncorrelated with the input signal and has only little power in the signal band. The system has been simulated assuming a 0.1% capacitor mismatch, and the achieved SNDR performance was 100 dB for an oversampling ratio of 7.

1. INTRODUCTION

High-performance digital-to-analog converters (DACs) are used for a variety of portable applications, e.g. in audio equipment. The signal-to-noise-and-distortion ratio (SNDR) is often required to be as large as 90–100 dB, a level of performance which cannot be obtained by brute-force implementation of DACs that rely on accurate matching of electrical parameters.

Error-shaping DACs have become popular because they facilitate linear D/A conversion despite the mismatch of electrical parameters [1–3]. In this way, expensive laser trimming and elaborate background-calibration techniques can be avoided.

Portable equipment requires the power consumption be low, and pseudo-passive DACs are potentially well suited for such applications. A pseudo-passive DAC containing only two capacitors, a reference voltage source, and a few switches (Fig. 1) was described by Suarez et al. [4]. It functions by repeatedly charging C_1 to V_{ref} or 0 depending on the incoming bits $x(n,k)$ and sharing the charge between C_1 and C_2. It requires N clock cycles to convert an N-bit digital word $x(n)$ into an analog voltage $y(n)$. A major disadvantage of this circuit is that its linearity is limited by the matching of the two capacitors, which is typically no better than 10 to 11-bit accurate. Several recent papers [5, 6] discuss methods for reducing this nonlinearity, but the algorithms described in them require very complex logic and introduce new practical problems associated with the precise addition of the analog outputs. This paper will discuss simpler techniques by which the DAC errors can be reduced by error cancellation and/or mismatch shaping [7].

2. DAC ERROR ANALYSIS

The following analysis refers to the DAC shown in Fig. 1. Define $v(n,k)$ as the voltage across C_1 and C_2 in the k-th clock phase

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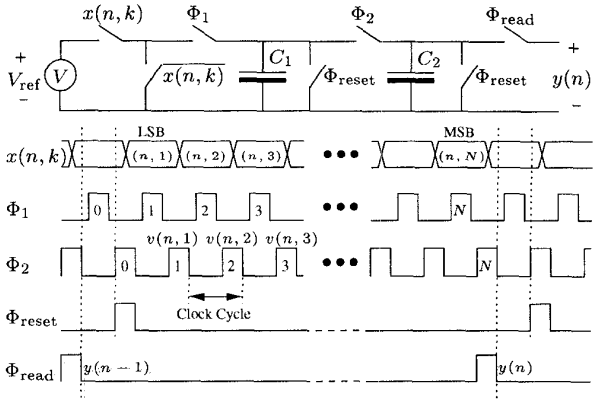

Figure 1: Basic two-capacitor DAC proposed by Suarez et al.

Φ_2. Each D/A conversion is initiated by a reset phase Φ_{reset}, thus $v(n,0) = 0$ for all n.

Just before the k-th clock phase Φ_2, capacitor C_2 will have the voltage $v(n,k-1)$, and capacitor C_1 will have the voltage $x(n,k)V_{\text{ref}}$. During clock phase Φ_2, charge sharing yields the following relation

$$v(n,k) = \frac{C_1}{C_1+C_2}x(n,k)V_{\text{ref}} + \frac{C_2}{C_1+C_2}v(n,k-1) \quad (1)$$

By introducing the mismatch parameter

$$\delta = \frac{C_{11}-C_{12}}{C_{11}+C_{12}} \quad (2)$$

eqn. (1) can be brought to the form

$$\begin{aligned} v(n,k) &= \frac{1+\delta}{2}x(n,k)V_{\text{ref}} + \frac{1-\delta}{2}v(n,k-1) \\ &= \frac{x(n,k)V_{\text{ref}} + v(n,k-1)}{2} \\ &\quad + \frac{\delta}{2}\left[x(n,k)V_{\text{ref}} - v(n,k-1)\right] \end{aligned} \quad (3)$$

The first term in eqn. (3) represents the ideal operation

$$y_{\text{ideal}}(n) = v_{\text{ideal}}(n,N) = V_{\text{ref}}\sum_{k=1}^{N} x(n,k)2^{k-N-1} = V_{\text{ref}}x(n) \quad (4)$$

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The second term represents the error caused by capacitor mismatch. For all practical purposes, it is sufficient to consider only the first-order errors[1], in which case $\delta v(n, k-1)$ can be approximated by $\delta V_{\text{ref}} \sum_{j=1}^{k-1} x(n,j)2^{j-k}$. This leads to the following evaluation of the error signal

$$\begin{aligned} e(n) &= y(n) - y_{\text{ideal}}(n) \\ &= \delta \cdot V_{\text{ref}} \sum_{k=1}^{N} \left[x(n,k) - \sum_{j=1}^{k-1} x(n,j)2^{j-k} \right] 2^{k-N-1} \end{aligned} \quad (5)$$

Notice that the main sum in eqn. (5) is a function of $x(n)$ only, i.e., $e(n)$ contains the harmonics of $x(n)$. The total harmonic distortion (THD) can, in principle, be calculated analytically except for the unknown parameter δ, to which the THD is proportional. Because an analytical expression will provide hardly any valuable insight, the THD performance was evaluated on the basis of simulations. It was found that, for a full-scale sinusoid input, the THD is approximately $(-5 + 20\log_{10}|\delta|)$ dB. Unfortunately, even when using the best known layout techniques, δ cannot be made much smaller than 0.1%, corresponding to only about 11-bit linearity.

3. MISMATCH-SHAPING DAC

The DAC's signal-band performance can be improved dramatically by using mismatch shaping. To obtain this behavior, the error signal $e(n)$ must be made uncorrelated with $x(n)$ (i.e., $e(n)$ must be a pseudo-noise signal), and its spectral power density must be suppressed in the signal band.

In most mismatch-shaping DACs the error signal is controlled by interchanging nominally identical components. For the two-capacitor DAC, the only degree of freedom is the choice of which capacitor (C_1 or C_2) is charged in clock phases Φ_1. A new choice can be made in every clock cycle. In the following, $t(n,k) = 1$ will represent the condition that C_1 is charged in the k-th clock cycle of the n-th sample, whereas $t(n,k) = -1$ will represent that C_2 is charged instead.

By revisiting eqns. (1–5), it is found that the error signal can be calculated from

$$\begin{aligned} e(n) &= \delta V_{\text{ref}} \sum_{k=1}^{N} t(n,k) b(n,k) 2^{k-N-1} \\ &= \delta V_{\text{ref}}\, \widehat{\epsilon}(n) \end{aligned} \quad (6)$$

where

$$b(n,k) = x(n,k) - \sum_{j=1}^{k-1} x(n,j)2^{j-k} \quad (7)$$

Notice that $e(n)$ is proportional to

$$\widehat{\epsilon}(n) = \sum_{k=1}^{N} t(n,k) b(n,k) 2^{k-N-1} \quad (8)$$

and hence that the error signal's spectral composition can be controlled without knowing the actual capacitor mismatch δ. In other words, the task is to choose $t(n,k)$ such that the spectral composition of $\widehat{\epsilon}(n)$ is of the desired form. A very simple error-canceling DAC will be discussed first.

[1] In other words, the terms that contain a coefficient δ^p, where $p > 1$, may be neglected.

3.1. Error-Canceling DAC

From eqn. (7) it can be observed that the coefficients $b(n,j), j \in \{1, 2, 3, \ldots, N\}$ are functions of the digital word $x(n)$ only. Eqn. (6) shows that, for a fixed $x(n)$, the polarity of $\widehat{\epsilon}(n)$ can be alternated by inverting $t(n,k), \forall k$. Hence, if $x(n)$ is D/A converted twice using opposite but otherwise arbitrary values for $t(n,k)$ in the two conversions, the two generated analog voltages $y_a(n)$ and $y_b(n)$ will include errors $e_a(n)$ and $e_b(n)$ of the same magnitude, but of opposite polarity. By adding or averaging $y_a(n)$ and $y_b(n)$, the result will be a first-order error-free D/A conversion.

Active circuitry will be required to add $y_a(n)$ and $y_b(n)$, but scaled averaging can be implemented passively as shown in Fig. 2. For simplicity, $t(n,k) = 1, \forall k$ in the first conversion Φ_a, and consequently $t(n,k) = -1, \forall k$ in the second conversion Φ_b. It can be shown that, despite mismatch of the nominally identical averaging capacitors C_a and C_b, only second- and higher-order mismatch errors $\delta^p, p > 1$, will affect $y(n)$.

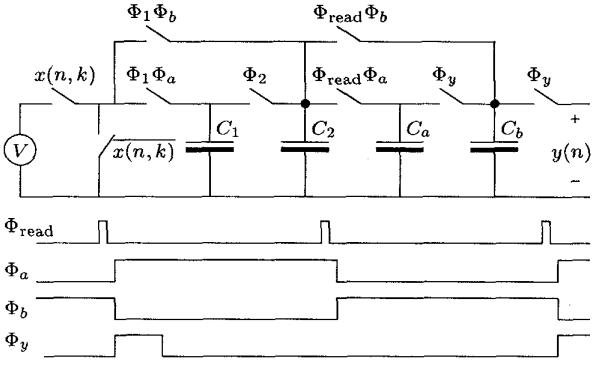


Figure 2: Error-canceling D/A converter that requires $2N$ clock cycles for the D/A conversion of a N-bit digital word $x(n)$.

The main disadvantage of the described error-canceling DAC is that $2N$ clock cycles are required for the D/A conversion of an N-bit digital word $x(n)$. If bandwidth is a problem, $x(n)$ can be interpolated to (say) $N/2$ bits of resolution using a low oversampling ratio of (say) 10 [8]. Notice that, to simplify the reconstruction filter processing $y(n)$, this degree of oversampling is generally required anyway.

The performance of the proposed system, using $\Delta\Sigma$ interpolation, is equivalent to that of a mismatch-shaping DAC, although the filtered pseudo-noise error signal is caused by the interpolation rather than capacitor mismatch.

3.2. Mismatch-Shaping Switching

The operation of the two-capacitor DAC can be made mismatch-shaping by choosing $t(n,k)$ appropriately in each clock cycle. An advantage of this approach, compared to the error-canceling approach, is that the two averaging capacitors C_a and C_b can be omitted and that only N clock cycles are required for the conversion of an N-bit word $x(n)$. The objective is to choose $t(n,k)$ such that $\widehat{\epsilon}(n)$ from eqn. (8) has the desired spectral composition.

Eqn. (7) shows that the coefficients $b(n,k)$ are functions of $x(n)$ only, and that $|b(n,k)| \leq 1$. Eqn. (8) shows that the set of values $\mathcal{E}[x(n)]$ that $\widehat{\epsilon}(n)$ can attain using all possible combinations

of $t(n,k)$ depends only, but strongly, on the coefficients $b(n,k)$, i.e., on $x(n)$[2]. Because $|b(n,k)| \leq 1$ and $|t(n,k)| = 1$, and because the $b(n,k)t(n,k)$ are scaled by 2^{k-N}, it follows that the values in $\mathcal{E}[x(n)]$ will be affected mainly by the most significant bits of $x(n)$.

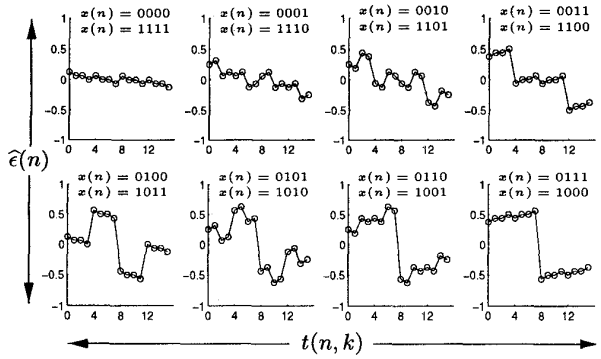


Figure 3: $\widehat{\epsilon}(n)$ as a function of the 4 MSBs of $x(n)$ and $t(n)$

Fig. 3 shows the attainable values of $\widehat{\epsilon}(n)$ for all combinations of $x(n)$ and $t(n,k)$ when represented with 4-bit accuracy. Eqn. (8) was approximated by a summation from $k = N-3$ to $k = N$, and in eqn. (7) $x(n)$ was approximated by xxxx10000 . . . . The horizontal axes represent the binary value of the 4 MSBs of $t(n,k)$. The sets $\mathcal{E}[x(n)]$ are found by projecting these values onto the vertical axes. Clearly, $\widehat{\epsilon}(n)$ is a highly nonlinear function of $x(n)$ and $t(n,k)$. The important point is, however, that the function is entirely numerical and independent of the capacitor mismatch δ. Hence, $\widehat{\epsilon}(n)$ can be controlled by choosing the sequence $t(n,k)$ according to the present value $x(n)$ and the desired value $\epsilon^*(n)$ of $\widehat{\epsilon}(n)$.

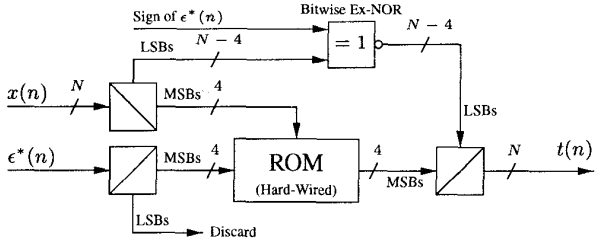


Figure 4: Sign selector choosing $t(n,k)$ such that $\widehat{\epsilon}(n)$ will attain a value close to $\epsilon^*(n)$.

Fig. 4 shows how the control system, which will be called a sign selector, can be implemented. The four MSBs of $t(n)$, i.e., $t(n,k)$ for $k \in \{N-3, N-2, N-1, N\}$ are selected on the basis of Fig. 3 as the code that yields the value of $\widehat{\epsilon}(n)$ which is the closest to $\epsilon^*(n)$ truncated to 4-bit representation. This operation can, for example, be implemented by four small 4x4 bit hard-wired read-only memories (a gate array). The LSBs of $t(n)$, i.e., $t(n,k)$ for $k \in \{1, 2, \ldots, N-4\}$ are chosen of the same/opposite polarity as that of the respective $b(n,k)$ coefficients, such that $\sum_{k=1}^{N-4} t(n,k)b(n,k)$ will have the same polarity as that of $\epsilon^*(n)$. This can be implemented by performing exclusive-NOR operations on $x(n,k)$ and the sign bit of $\epsilon^*(n)$ (which is assumed to be logic 1 when $\epsilon^*(n)$ is positive).

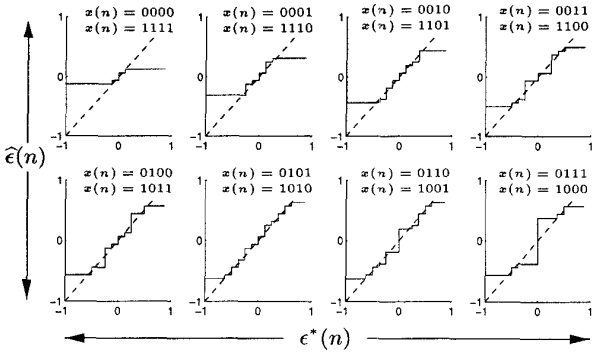


Figure 5: Control characteristic of $\widehat{\epsilon}(n)$ as a function of $\epsilon^*(n)$.

Fig. 5 shows the sign selector's control characteristic, i.e., the relation between $\epsilon^*(n)$ and $\widehat{\epsilon}(n)$, when the sign selector is implemented as shown in Fig. 4. Clearly, the controllability of $\widehat{\epsilon}(n)$ and the control characteristic's linearity depends on the digital input word $x(n)$; this reflects the composition of $\mathcal{E}[x(n)]$. The controllability of $\widehat{\epsilon}(n)$ is, however, much better than that of a traditional single-bit $\Delta\Sigma$ modulator (Fig 6) where $\widehat{\epsilon}(n)$ can attain only two values $x(n) - 1$ and $x(n) + 1$, neither of which necessarily will be close to $\epsilon^*(n)$.

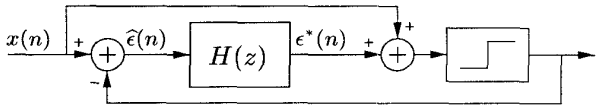


Figure 6: $\Delta\Sigma$ modulator showing the equivalents of $\widehat{\epsilon}(n)$ and $\epsilon^*(n)$.

Fig. 7 shows a block diagram of the overall DAC system. The $\Delta\Sigma$ modulator can be implemented using serial logic because it is clocked only once for each new sample $x(n)$.

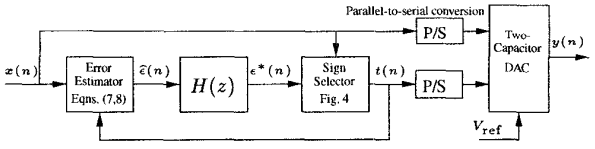


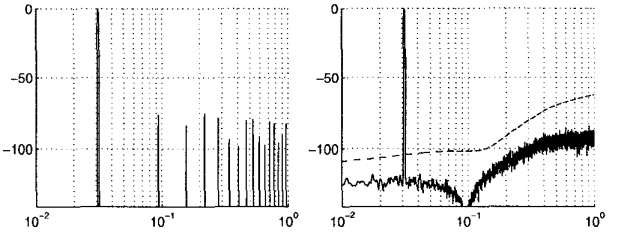
Figure 7: Mismatch-shaping two-capacitor DAC system.

The sign selector, shown in Fig. 4, can be simplified by reducing the ROM's resolution, but the corresponding control characteristic will typically be less linear. In the extreme case, the ROM

[2]This property is shared by single-bit $\Delta\Sigma$ modulators, where $\mathcal{E}[x(n)]$ is a set of only two values: $x(n) - 1$ and $x(n) + 1$. For the two-capacitor DAC, however, $\mathcal{E}[x(n)]$ may contain as many as 2^N elements grouped in pairs of equal value but opposite polarity.

may be entirely omitted, and then the control characteristic will resemble that of a single-bit delta-sigma modulator. The linearity required of the control characteristic depends on how aggressively the loop filter $H(z)$ is designed. If the control characteristic is very nonlinear the maximum gain $\mathrm{NTF}_{\max}$ of the noise transfer function's $\mathrm{NTF}(z) = 1/(1 + H(z))$ should be less than (say) 1.5 [1]. However, if the control characteristic is fairly linear, $\mathrm{NTF}_{\max}$ may be chosen larger, and the signal-band suppression of $\hat{\epsilon}(n)$ will be improved [8].

The loop filter $H(z)$ need not be of high order because the Nyquist-band error power is low (in the order of -60 dB). Considering that the control characteristic is always quite nonlinear for low-level inputs, i.e., when the MSBs of $x(n)$ is "1000" or "0111," it makes good sense to use a simple (second-order) loop filter because it always will be stable[3].



(a) dB vs. $2f/f_s$ (b) dB vs. $2f/f_s$

Figure 8: Simulated (FFT) performance of the DAC without (a) and with (b) mismatch shaping using a second-order loop filter $H(z)$.

Fig. 8 shows the simulated performance when the relative capacitor mismatch was 0.1%. The peak-to-peak value of $y(n)$ was $0.71V_{\mathrm{ref}}$, which is defined as 0 dB. Fig. 8a shows the performance of the basic DAC shown in Fig. 1. Harmonic spurs are observed; the THD performance is approximately -71 dB. Fig. 8b shows the performance of the mismatch-shaping DAC shown in Fig. 7, for which $\mathrm{NTF}(z) = 1 - 1.91z^{-1} + z^{-2}$ and a small amount of dither was added to $\epsilon^*(n)$ to prevent idle tones. Harmonic spurs are not observed, and the mismatch-shaping property is observed. The error signal's signal-band power is shown as the dashed line; the performance is better than 100 dB even for oversampling ratios as low as 7.

4. CONCLUSIONS

The discussed pseudo-passive two-capacitor DAC structure is suitable for portable applications because it uses only little dc power. The serial operation limits the bandwidth, but it is wide enough for audio application, for example. Two techniques were proposed to avoid the harmonic distortion caused by capacitor mismatch. The error-canceling DAC, shown in Fig. 2, is simple to implement and will yield a very good performance. The bandwidth-to-power ratio, however, is cut in half because each digital word is converted twice.

[3]Higher-order loop filters can designed and successfully used, but it is advisable to stabilize the $\Delta\Sigma$ modulator by hard-limiting the state variables representing higher-order summations of $\hat{\epsilon}(n)$, or by incorporating reset operations when the system becomes unstable.

To avoid very complex reconstruction filters, most DACs will convert somewhat oversampled signals. Even if the oversampling ratio is as low as 7 to 10, 100 dB signal-band performance can be obtained when using the mismatch-shaping DAC shown in Fig. 7. It requires more digital circuitry, but even so, the overall power consumption may be lower than that of the error-canceling DAC. If the loop filter is of low order, the control characteristic may be quite nonlinear and the sign selector can be made very simple. The operation is based on a mathematical estimate of the capacitor mismatch error that is accurate to a first-order approximation. Other higher-order errors not accounted for are essentially negligible.

Although not discussed in this paper, the two-capacitor DAC can be made insensitive to charge-injection and clock-feedthrough errors [9].

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